

Benjamin Sirota

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EDUCATION

The University of Pennsylvania MSE Electrical Engineering GPA: 3.7/4.0 Concentrations: Computer Engineering and Embedded Systems	Philadelphia PA December 2026
The George Washington University B.S. Computer Engineering	Washington DC May 2025

TECHNICAL SKILLS

- **Programming Languages:** C, C++, Python, Java, Javascript, MATLAB, Verilog, SystemVerilog, Linux/Shell Scripting, TCL
- **CAD Software:** Solidworks, Fusion 360, Onshape, AutoCAD, Altium Designer, KiCad
- **EDA Software:** Multisim, Vivado, KLayout, Cadence Virtuoso, Innovus, Synopsys Design Compiler, TetraMAX, Vitis HLS
- **Fabrication Techniques:** Mill, Lathe, TIG Welder, 3D Printing, Laser Cutting, Micro/Nanofabrication, SEM

EXPERIENCE

The George Washington University ECE Department Student Teaching Assistant	Washington DC August 2023 - May 2025
<ul style="list-style-type: none">• Fulfilled undergraduate teaching assistant responsibilities by holding regular office hours, tutoring students, and co-leading laboratory sessions for foundational ECE courses (Circuit Theory, Engineering Electronics, C Programming, Data Structures).	
The George Washington University Information Technology Student Technical Specialist Level 3	Washington DC October 2023 - May 2025
<ul style="list-style-type: none">• Provided university-wide Tier 1 IT support, independently resolving routine technical tickets via phone and email.• Triaged and escalated advanced system and network issues to specialized higher-level support tiers to ensure rapid incident resolution.	

PROJECTS

GW Baja SAE Captain (2024-2025) Head of Design/Suspension (2023-2024)	September 2021 - June 2025
<ul style="list-style-type: none">• Established the team as an official university student organization and led the design and manufacture of an off-road racing vehicle for the Baja SAE program.• Fabricated custom vehicle components by operating advanced machining tools, including a manual lathe, manual mill, Haas CNC mill, and TIG welder.	
Raytheon Autonomous Vehicle Competition Communications Subteam Lead	Spring 2024 - Spring 2025
<ul style="list-style-type: none">• Designed and manufactured two UAVs (Unmanned Aerial Vehicles) to compete in Raytheon Autonomous Vehicle Competition <i>Operation Full Send</i>• One UAV scans and identifies markers within a field, while the other UAV delivers a package to one of the identified markers• Led a team of 5 members to design a system to communicate navigation coordinates, status, and logs over WiFi and RF between two UAVs	
USB Art-Net DMX Controller	Summer 2026
<ul style="list-style-type: none">• Designed and routed a custom PCB, integrating an ESP32-S2 microcontroller with isolated DC-DC power and XLR3 DMX connectivity.• Developed embedded C firmware using the ESP-IDF framework to implement Art-Net/DMX communication protocols and a USB NCM interface for data routing.	

32-Channel Live Theater Audio Mixer

Summer 2026 (In Progress)

- Architecting a custom 32-channel digital audio mixer targeting live theater applications.
- Designing a mixed-signal PCB integrating ADC/DAC stages, power management, and an ESP32-S3 microcontroller.
- Developing a TDM audio processing pipeline and SPI communication interface in SystemVerilog for a Cmod-A7 FPGA.
- Writing C firmware to manage system routing and the user interface.

FPGA Ethernet Data Compression Pipeline

Fall 2025

- Engineered a high-throughput Ethernet data compression system on an Ultra96 FPGA board, achieving processing speeds of 100Mb/s.
- Developed the system architecture in C++ utilizing High-Level Synthesis (HLS) to leverage FPGA acceleration, parallel processing, and extensive pipelining.
- Designed a comprehensive data processing pipeline featuring Content-Defined Chunking (CDC), SHA Hashing, Data Deduplication, and LZW Compression.

IoT Smart Chicken Coop

Spring 2026

- Developed an automated, WiFi-connected environmental control system using an SiWg917 network processor.
- Engineered a fully custom PCB to route electrical components and integrate temperature, humidity, air pressure, ambient light, and PIR motion sensors.
- Programmed custom logic to autonomously trigger door actuators and feeders based on configurable environmental metrics and remote manual inputs.

8-Bit Pipeline ADC

Spring 2026

- Designed an 8-bit Pipeline Analog-to-Digital Converter (ADC) capable of operating at a >2MHz sampling frequency using Cadence Virtuoso and an AMI 0.6μ process.
- Engineered Switched-Capacitor Multiplying DAC (MDAC) circuits for residue amplification and implemented sub-DACs utilizing resistive elements.
- Characterized static (INL/DNL) and dynamic (SNDR, SFDR, ENOB) performance, optimizing for minimal power dissipation to maximize the Figure of Merit (FOM).

RV32IM Pipelined Processor

Spring 2026

- Developed a fully functional RISC-V processor in SystemVerilog, successfully implementing the complete RV32IM Instruction Set Architecture (ISA), and tested on an FPGA.
- Architected and integrated a classic 5-stage instruction pipeline to optimize instruction throughput and overall processor efficiency.

PennOS (Unix-Like Operating System)

Summer 2026

- Developed an interactive shell supporting multi-process pipelines, standard I/O redirection, and foreground/background job control using process group isolation.
- Engineered a FAT16-like file system within a single host file, implementing FAT chain traversal, block allocation, and a kernel-level open file table.
- Architecting a priority-based process scheduler and kernel-level system calls to manage context switching, file descriptors, and process states.

Biometric Attendance System

Fall 2025

- Engineered an automated classroom attendance tracking system utilizing an ATmega328PB microcontroller, a fingerprint sensor, and an LCD interface.
- Collaborated in a 3-person team to develop secure biometric check-in/out functionality, streamlining the daily recording process.
- Implemented data logging capabilities to securely store and append student ID records directly onto an SD card for instructor access.

AES-128 Cryptographic Accelerator

Spring 2025

- Implemented a complete AES-128 encryption core using Verilog for secure, hardware-accelerated data processing.
- Executed the physical design flow utilizing Cadence Innovus for precise chip layout, placement, and routing.
- Optimized the synthesized logic to achieve an ideal balance between physical die area and processing speed.

SPI Memory Controller

Fall 2024

- Authored a Serial Peripheral Interface (SPI) controlled memory module in Verilog.
- Designed the digital interface to successfully decode incoming SPI signals from a host microcontroller for reliable word storage and retrieval.

RELEVANT COURSEWORK

Undergraduate: VLSI Design and Simulation, Design of VLSI Circuits, ASIC Design and Testing, Computer Architecture and Design, Micro/Nanofabrication Technology, Digital Design with FPGAs, Analog Electronics Design, Digital Electronics Design, Embedded Systems, Digital Signal Processing, Computer Networks, Software Engineering

Graduate: Smart Devices, IoT Edge Computing, System-on-a-Chip Architecture, Computer Organization and Design, Operating Systems, Digital Integrated Circuits and VLSI-Fundamentals, Mixed Signal Circuit Design and Modeling, IoT Wireless, Security, & Scaling, Operating Systems Design and Implementation, Design of Mechatronic Systems